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EXAMINER	
JAGANNATHAN, MELANIE	
ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/334,693	Applicant(s) LAU ET AL.	
	Examiner Melanie Jagannathan	Art Unit 2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-14,23-26 and 34-37* is/are rejected.

7)☒ Claim(s) *5-11,15-22,27-33,38-44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims **1-4, 12-14, 23-26,** and **34-37** are rejected under 35 U.S.C. 102(e) as being anticipated by Sato U.S. Patent Number 6,128,318.

Regarding claims **1,12,23,34**, the claimed maintaining a synchronization state of a number of components of a distributed system is anticipated by method of synchronizing a "global" cycle master node (Figure 1, element 22) to cycle slave nodes (element 20) in a network. See column 1, lines 35-39 and lines 66-67, column 2, line 1 and column 4, lines 7-14. The claimed synchronization according to a number local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components is anticipated by cycle reset signal asserted at a prescribed rate which is a multiple of one cycle of the cycle slave node and all of the cycle slave nodes are synchronized to the cycle reset signal.

See column 3, lines 3-8. The claimed local clock generating circuit synchronized to the global synchronization signal is anticipated by each cycle slave node including its own cycle clock subsystem (Figure 1, element 27) which includes a clock timer (element 30) and each of the cycle slave nodes are synchronized to the cycle timer (element 38) of the cycle master node (element 22). See column 4, lines 7-14.

Regarding claims **2,13,24,35**, the claimed entering of synchronization state only after observing a predetermined number of successive local clock cycles between successive occurrences of global synchronization signal is anticipated by cycle reset signal asserted at a prescribed rate which is a multiple of one cycle of the cycle slave node and the cycle master node regularly distributes its cycle timer value to all of the other cycle slave nodes in the network so all cycle timers of the cycle slave nodes are synchronized to the cycle timer of the cycle master slave node and the cycle timer value of the cycle master node is synchronized to the cycle reset signal, thus keeping all of the cycle timers in the slave nodes synchronized to the reset signal. See column 4, lines 7-21 and column 5, lines 54-60.

Regarding claims **3,25,36**, the claimed local clock generating circuit providing local control signals is anticipated by method, in response to cycle reset signal asserted at a rate multiple of one cycle, utilizing logic circuitry in the cycle slave node to determine a timer offset value and using this value to adjust a value of a cycle master node cycle timer (element 38).

Regarding claims **4,14,26,37**, the claimed local clock generating circuit providing local control signals even after an instance of the global synchronization signal is observed at time instant corresponding to one local clock cycle more or less than the number of clock cycles is anticipated by in response to cycle reset signal asserted at a rate multiple of one cycle, utilizing

logic circuitry in the cycle slave node to determine a timer offset value and using this value to adjust a value of a cycle master node cycle timer (element 38).

Allowable Subject Matter

3. Claims **5-11, 15-22, 27-33,** and **38-44** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed May 9, 2003 have been fully considered but they are not persuasive. Examiner appreciates detailed description of prior art Sato.

Applicant argues reference Sato does not teach a number of local clock cycles recorded between successive occurrences of a global synchronization signal provided to each of the components. Examiner contends the cycle reset signal is asserted at a prescribed rate, which is a multiple of one cycle of the cycle slave node, and all of the cycle slave nodes are synchronized to the cycle reset signal. See column 3, lines 3-8.

Applicant argues reference Sato does not disclose the claimed local clock generating circuit being synchronized to the global synchronization signal. Examiner contends each cycle slave node includes its own cycle clock subsystem (Figure 1, element 27) which includes a clock timer (element 30) and each of the cycle slave nodes are synchronized to the cycle timer (element 38) of the cycle master node (element 22) which is synchronized to the cycle reset signal. See column 4, lines 7-14 and column 5, lines 54-60.

Therefore, prior art rejection is proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melanie Jagannathan whose telephone number is 703-305-8078. The examiner can normally be reached on Monday-Friday from 8:00 a.m.-4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 703-308-5463. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9315 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Melanie Jagannathan
Patent Examiner
AU 2666

MJ
July 2, 2003

DANG TON
PRIMARY EXAMINER